

## Designing a low-noise VCO on FR4

*Using a CAD program, you can design a cost-effective voltage controlled oscillator using inexpensive PWB materials.*

By Randall W. Rhea

Although FR4 material and process handling are widely available, the poorly controlled dielectric constant and high-loss tangent challenge the design of high performance circuits. This article illustrates the use of modern computer aided design (CAD) techniques and provides tips on the design of a 900 MHz voltage controlled oscillator (VCO). It has a high tolerance to FR4 material and -100 dBc/Hz SSB phase-noise at 10 kHz offset. The techniques and tips are also applicable to other circuitry, such as filters and amplifiers.

### FR4 material

FR4 is a flame-retardant version of G10. Both are thermoset fiberglass epoxy laminates. The resin has a relative dielectric constant of 3.4, the glass has a dielectric constant of 6.1. These figures represent the extreme range of possible dielectric constants. A typical board has a resin content from 40% to 70% for a dielectric constant range of 4.2 to 4.9. Dielectric constant variations of  $\pm 0.06$  across the sheet is common.

The loss tangent of FR4 is typically 0.008 at VHF frequencies and 0.02 at

microwave frequencies. This is an unloaded material Q of 125 to 50, which is adequate to support lowpass filters, broadband bandpass filters and many oscillators. Edge-coupled, hairpin and interdigital filters, have resonate quarter wavelength open ends with high field intensity and are not a good choice for filters on FR4. On the other hand, combine filters replace this end with loading capacitance. The remaining shorted length of line has high current but low field intensity, reducing the effect of dielectric loss and dielectric constant variation. This technique is used in designing the resonator for this VCO.

The VCO specifications are:

Frequency:	890-910 MHz
Pout:	7±1 dBm
Harmonics:	< -10 dBc
Vsupply:	9.7 Vdc nominal
Vtune:	2-13 Vdc maximum
Isupply:	40 mA maximum
SSB phase-noise:	95 dBc @ 10 kHz offset
Size:	1x1 inch maximum

The VCO will be phase-locked to 900 MHz. The expanded frequency range covers temperature variation. Excessive tuning range is avoided to minimize

varactor noise.

### Initial considerations

The output power, harmonic level and power supply specifications are unremarkable and are typical of systems with ample supply power. The design is driven by the phase-noise specification, the characteristics of FR4 and the narrow tuning range (2.2%). Circuit performance is based on satisfying fundamental criteria and circuit complexity is seldom helpful. In this case, low cost is achieved with a straightforward oscillator topology: a Mini-Circuits MAR-3 MMIC amplifier, a resonator printed on FR4 and few supporting components.

SSB phase-noise is predicted by Leeson's equation [1]

$$L(f_m) = 10 \log \left[ \frac{1}{2} \left( \frac{f_c}{f_m} \right)^2 + 1 \right] \left( \frac{f_c}{f_m} + 1 \right) \left( \frac{F k T}{P_s} \right)$$

where:

- $f_0$  = carrier frequency
- $Q_l$  = oscillator loaded Q
- $f_m$  = carrier offset frequency
- $f_c$  = active device flicker corner frequency
- F = oscillator amplifier noise factor
- k = Boltzmann's constant
- T = operating temperature

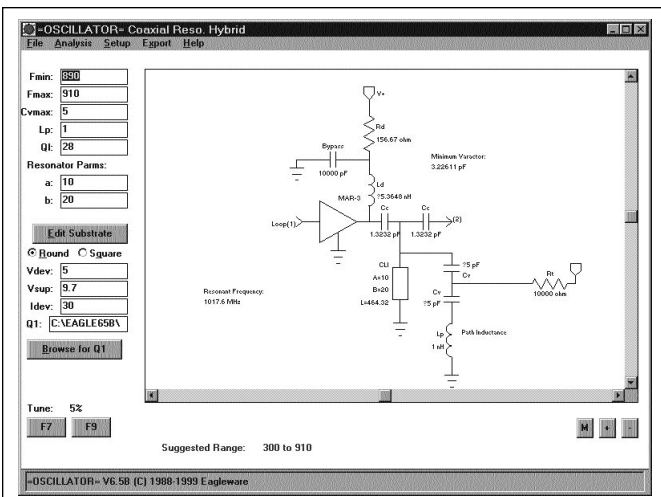


Figure 1. Initial oscillator design of the 900 MHz VCO in the =Oscillator= module of the Genesys software suite. Input parameters are given on the left and the design is displayed on the right.

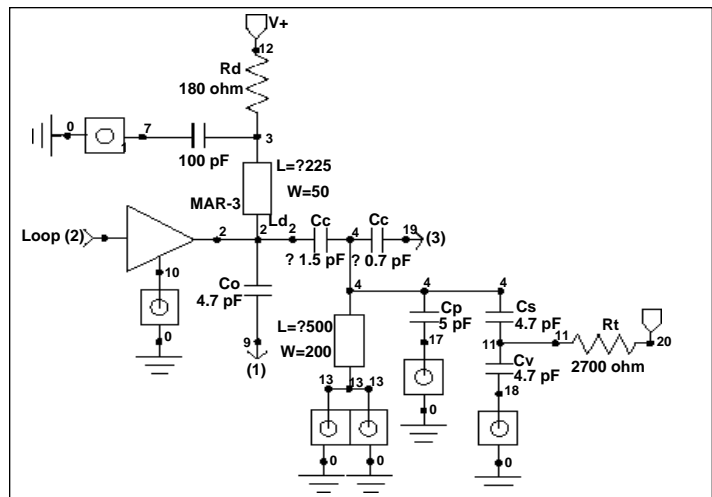


Figure 2. Schematic of the 900 MHz after the design modifications described in the text. The values with "?" were optimized by the =SuperStar= Genesys module to satisfy the open-loop criteria for the oscillator.

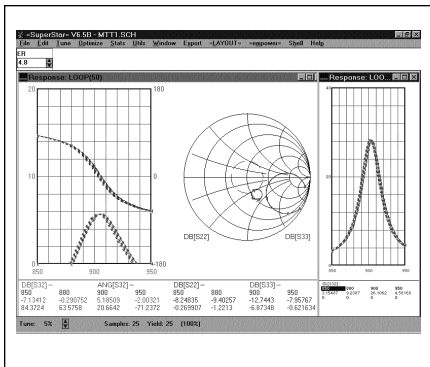


Figure 3. The open-loop responses and loaded Q of the VCO with a Monte Carlo analysis of FR4 dielectric constant variation of -2 to +10%. Notice the frequency variation is only about 3 MHz or 0.33%.

$P_s$  = oscillator power output

The oscillator's fundamental properties, under the designer's control, that impact phase-noise are amplifier noise figure, the output power and the loaded Q. The noise-figure difference between an inexpensive and state-of-the-art amplifier design is only a few decibels. More important is the output power, which can be increased indefinitely to achieve a desired phase-noise performance. However, the parameter with the strongest influence is loaded Q (second power rather than linear). To keep DC current consumption down the designer should concentrate on loaded Q to achieve the desired phase-noise. With an output power of +7 dBm and an MAR-3 noise figure of 6 dB, a loaded Q of 28 yields a SSB phase-noise of better than -100 dBc/Hz at 10 KHz offset, providing a few decibels of margin to the desired -95 dBc/Hz.

### The Design

The initial design is created using the

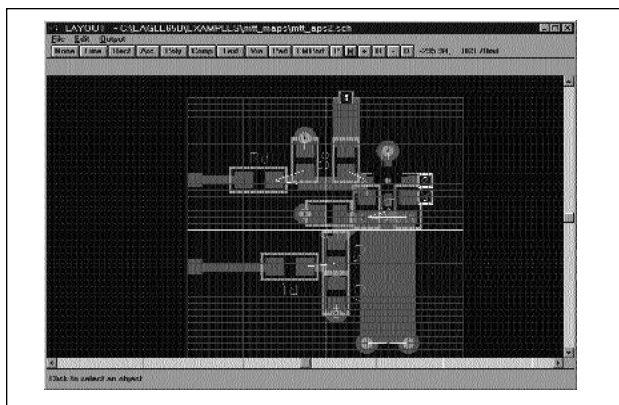


Figure 4. Layout of the VCO in the =Layout= module of Genesys. The output is taken at the top, power is supplied at the upper left and the tuning voltage is applied to the lower left.

=Oscillator= module of Genesys [2](a sample screen is shown in Figure 1). =Oscillator= uses the design parameters on the left to create the schematic shown on the right. The MAR-3 is defined by S-parameter data read from a industry-standard S2P file.

=Oscillator= used a ceramic-loaded TEM-mode coaxial resonator. These popular resonators achieve unloaded Qs as high as 1000. To minimize cost, this design will use a resonator printed on FR4 so I modified the =Oscillator= design as follows:

1) The coaxial resonator was replaced with a microstrip line. The effects of a poorly controlled dielectric were minimized by shortening the resonator to much less than quarter-wavelength and achieving resonance by loading with a lumped parallel capacitor ( $C_p$ ). The tuning varactor ( $C_v$ ) and its coupling capacitor ( $C_s$ ) also load the resonator. A quarter-wave resonator is inductive near the ground end and capacitive near the open end. The capacitive end is dominated by dielectric properties, the inductive end is not. Replacing the line's open-end section with lumped capacitance minimizes the impact of the FR4 dielectric.

2) For improved simulation accuracy the ideal grounds in the schematic were replaced with via hole models.

3) The inductor choke that supplies power to the MAR-3 was replaced with a printed microstrip line.

4) A capacitor ( $C_o$ ) was added to couple output power to a 50 ohm load.

The final schematic from the Genesys =Schemax= module is given in Figure 2. The oscillator design is characterized by an open-loop analysis from port 2 to port 3[3]. The resonator coupling capac-

itors, the length of the resonator microstrip line and the length of the power coupling choke microstrip line were optimized in the =SuperStar= circuit theory simulator. This step was taken to achieve a gain margin of at least 7 dB, a phase shift of 0 degrees at 900 MHz (this sets the oscillating frequency), matched impedances at the input and output and a loaded Q of at least 28. Figure 2 provides component values after optimization.

Figure 3 illustrates the open-loop plots after optimization with a Monte Carlo analysis with a dielectric constant variation of -2% to +10%. Notice the spread in the frequency of the phase zero-crossing is approximately 3 MHz or only 0.33%. The desensitizing to dielectric constant variation suggests the effects of dielectric loss are also minimized. Although the gain margin is slightly less than desired, a loaded Q of 28 was achieved and the matches are reasonable.

### Creating a layout

Figure 4 shows the layout in the Genesys module =Layout=. When =Layout= is launched it places metal on the workspace for each object in =Schemax=. Microstrip metal is automatically dimensioned to sizes set in the optimization and footprints are dropped for lumped elements. Originally, all of the metal and footprints are scattered in the workspace and connected together with rubber band lines. Figure 4 also illustrates the layout after rubber band lines have been resolved. Power is delivered to the circuit through Rd, the varactor tuning voltage through Rt and output is taken at port 1 through Co. Internal ports 2 and 3 are used for an

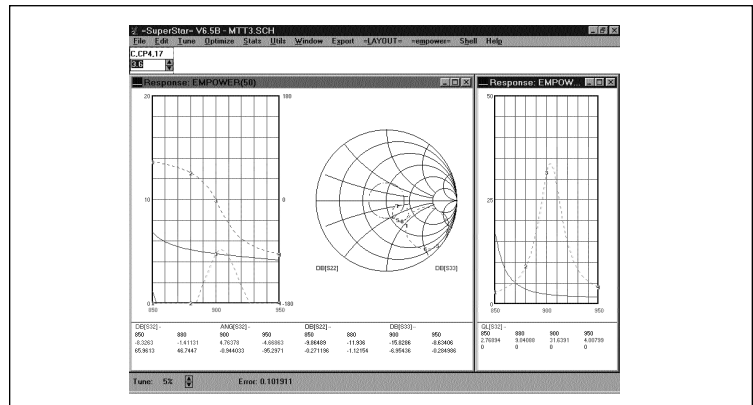


Figure 5. Oscillator open-loop responses computed by the Genesys electromagnetic program =Empower=. The solid traces are the original results and the dashed traces are after dropping  $C_p$  to 3.6 pF to correct the frequency.

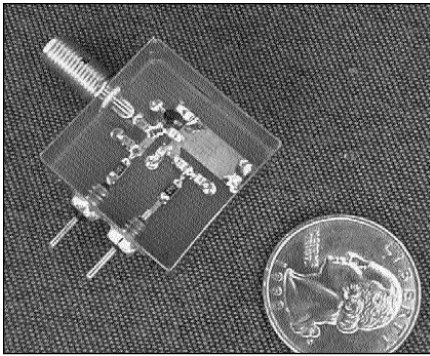


Figure 6. Completed VCO on FR4. The resonator is the large copper area on the right in the VCO.

electromagnetic analysis of the oscillator open loop. The oscillator is formed by bridging these ports with solder. =Layout= outputs AutoCad DXF files, Gerber files with an Excellon drill list and HPGL plotter files.

### Electromagnetic Analysis

An electromagnetic analysis was performed before constructing the oscillator. The pads of the loading, tuning

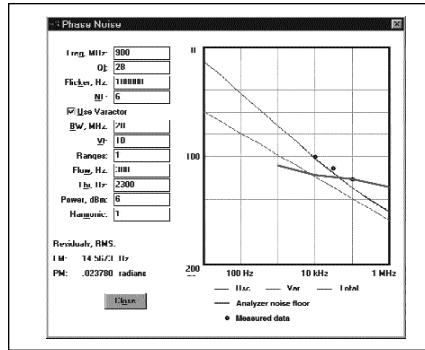


Figure 7. Predicted and measured (circles) VCO SSB phase-noise.

and coupling capacitors will add capacitance to ground. Additionally, other parasitic effects are likely to lower the oscillating frequency as well. The =Empower= module in Genesys will consider this, the cover and other packaging effects. =Empower= removes the lumped elements and replaces them with internal ports, performs a multiport analysis and then places the components back in the circuit.

=Empower= performs these tasks automatically on the user's behalf. Other advanced =Empower= features include multimode analysis and decomposition, generalized S-parameter analysis, automatic detection of four types of symmetry and loss calculation in both metal and dielectric. Results are shown in Figure 5.

The initial responses are solid and indicate that the frequency is lower than circuit theory simulation predicts. In the dashed responses the loading capacitance  $C_p$  was reduced to 3.6 pF to correct the frequency. This lower parallel capacitance compensates for the footprint pad capacitance at the top of the microstrip resonator.

### Measured data

A Gerber file from =Layout= was used with a Quick Circuit 5000 to machine a PWB. Bus wire feed-throughs were used for ground vias (a completed VCO is shown in Figure 6). With a Metelics MSV34-082 varactor in place of  $C_v$  the VCO tuned from 852 MHz with

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Vt= 0 V to 912 MHz with Vt= 12 V. The output level was +7.5 dBm with a fixed capacitor for Cv and +6.2 dBm with the varactor. The second harmonic was -28 dBc; the 3rd harmonic was -34 dBc. The current at 9.7 V was 30 mA. The measured frequency with a fixed capacitor for Cv was 887 MHz, well within the expected frequency range considering an electromagnetic simulation prediction of 903 MHz and tolerances in the lumped capacitors.

The measured SSB phase-noise is given in Figure 7 for offsets of 10, 30 and 100 KHz superimposed on the phase-noise predicted by the =Oscillator= Genesys module and the noise floor of the spectrum analyzer used to take the data. Close agreement was achieved.

### Concluding remarks

A number of issues associated with VCO design were illustrated using circuit theory and electromagnetic computer analysis and measured data. Quality performance is achievable on in-

expensive FR4 material. Quick and accurate design is possible using advanced integrated tools. Tools to automate and simplify electromagnetic analysis, which is more accurate than circuit theory analysis. Finally, there are simple fundamental concepts that can be used to control phase-noise performance as, predicted by Leeson's equation.

In this case a simple design was employed using an easily applied MMIC amplifier. However, it should be noted that an output power of +7 dBm is somewhat low for nearly 300 mW of DC supply consumption. A discrete one-transistor design could be used to achieve a lower amplifier noise figure, with less resistance in the collector-emitter path and a higher output power. This would result in improved phase-noise performance at the expense of a few more components for biasing the discrete device.

### References

[1] D.B. Leeson, "A Simple Model of Feedback Oscillator Noise Spectrum",

*Proc. of the IEEE*, February 1966, pp. 329-330.

[2] Synthesis Manual GENESYS Version 6.0, Eagleware Corporation, Tucker, Georgia, 1997.

[3] R.W. Rhea, *Oscillator Design and Computer Simulation*, 2nd edition, Noble Publishing, Atlanta, 1995.

### About the Author

Randy W. Rhea was an RF/microwave design engineer for 20 year with Boeing, Goodyear Aerospace and Scientific-Atlanta. In 1995 he founded Eagleware and later Noble Publishing. He can be reached at 770-939-0156.